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<u>L19</u>	L18 and (configur\$5 or reconfigur\$5)	505	<u>L19</u>
<u>L18</u>	L17 and (programmable or programable or eras\$5)	554	<u>L18</u>
<u>L17</u>	l3 and (array\$1 or matrix or matrices)	638	<u>L17</u>
<u>L16</u>	l5 and l8	1	<u>L16</u>
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<u>L14</u>	l5 and l6	15	<u>L14</u>
<u>L13</u>	L10 and l8	0	<u>L13</u>
<u>L12</u>	L10 and l7	1	<u>L12</u>
<u>L11</u>	L10 and l6	6	<u>L11</u>
<u>L10</u>	L9 and flash	238	<u>L10</u>

<u>L9</u>	(sram\$1 or dram\$1) and l5	288	<u>L9</u>
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<u>L8</u>	(716/13,14,17)![CCLS]	1217	<u>L8</u>
<u>L7</u>	(712/12-18,35-38)[CCLS]	1392	<u>L7</u>
<u>L6</u>	(712/2-300)[CCLS]	11509	<u>L6</u>
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<u>L5</u>	L4 and (configur\$5 or reconfigur\$5)	653	<u>L5</u>
<u>L4</u>	L3 and (programmable or programable or eras\$5)	749	<u>L4</u>
<u>L3</u>	L1 and (analog or digital) near4 (cell\$1 or block\$1)	936	<u>L3</u>
<u>L2</u>	L1 and (analog or digital) near4 (cell\$1 oe block\$1)	1231	<u>L2</u>
<u>L1</u>	(non near1 volatile) and microcontroller\$1	9180	<u>L1</u>

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1. Soft-defect detection (SDD) technique for a high-reliability CMOS SRAM
Kuo, C.; Toms, T.; Neel, B.T.; Jelemensky, J.; Carter, E.A.; Smith, P.;
Solid-State Circuits, IEEE Journal of
Volume 25, Issue 1, Feb. 1990 Page(s):61 - 67
Digital Object Identifier 10.1109/4.50285
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**1. Architecture of a mixed mode fuzzy controller**

Ungerling, A.P.; Herbst, D.; Weyergraf, A.; Goser, K.;
Fuzzy Systems, 1995. International Joint Conference of the Fourth IEEE International Conference on
The Second International Fuzzy Engineering Symposium., Proceedings of 1995 IEEE International
Volume 3, 20-24 March 1995 Page(s):1191 - 1196 vol.3
Digital Object Identifier 10.1109/FUZZY.1995.409834

[AbstractPlus](#) | Full Text: [PDF](#)(312 KB) IEEE CNF**2. Approaching evolvable hardware to reality: The role of dynamic reconfiguration and virtual**

Moreno, J.M.; Cabestany, J.; Madrenas, J.; Canto, E.; Faura, J.; Insenser, J.M.;
Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999. MicroNeuro '99. Proceedings of
International Conference on
7-9 April 1999 Page(s):163 - 170
Digital Object Identifier 10.1109/MN.1999.758860

[AbstractPlus](#) | Full Text: [PDF](#)(236 KB) IEEE CNF**3. Electronic converter for the analysis of photovoltaic arrays and inverters**

Sanchis, P.; Echeverria, I.; Ursua, A.; Alonso, O.; Gubia, E.; Marroyo, L.;
Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual
Volume 4, 15-19 June 2003 Page(s):1748 - 1753 vol.4
Digital Object Identifier 10.1109/PESC.2003.1217720

[AbstractPlus](#) | Full Text: [PDF](#)(1003 KB) IEEE CNF**4. Incorporating self-testing capabilities into a systolic array cell for digital signal processing**

Chen, C.-I.H.; Smith, R.;
Systems Engineering, 1990., IEEE International Conference on
9-11 Aug. 1990 Page(s):240 - 243
Digital Object Identifier 10.1109/ICSYS.1990.203142

[AbstractPlus](#) | Full Text: [PDF](#)(344 KB) IEEE CNF**5. Low floor trams with IGBT-3-level Inverter**

Schutze, T.; Stronisch, V.;
Power Electronics and Applications, 1993., Fifth European Conference on
13-16 Sep 1993 Page(s):92 - 96 vol.6

[AbstractPlus](#) | Full Text: [PDF](#)(220 KB) IEEE CNF**6. A VLSI inner product macrocell**